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DATE MAILED: 03/14/2006

APPLICATION NO).	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,184		04/02/2004	David L. Linam	AG10031083-1	2153
22878	7590 03/14/2006			EXAMINER	
		NOLOGIES, INC.	LAM, TUAN THIEU		
		ROPERTY ADMIN	1271277	2.000.000	
P.O. BOX	7599			ART UNIT	PAPER NUMBER
M/S DL42	9		2816		
LOVELA	ND, CO	80537-0599			

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
Office Action Summary		10/817,184	LINAM ET AL.				
		Examiner	Art Unit				
		Tuan T. Lam	2816				
	he MAILING DATE of this communication app	ears on the cover sheet with the c	orrespondence address				
	Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1)⊠ Re	esponsive to communication(s) filed on <u>09 Fe</u>	ebruary 2006.					
· ·	· · · · · · · · · · · · · · · · · · ·	action is non-final.					
3)☐ Sir	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
clo	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4)⊠ Cla	4)⊠ Claim(s) <u>9-16</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.							
5)∏ Cla	aim(s) is/are allowed.						
6)⊠ Cla	aim(s) <u>9-16</u> is/are rejected.						
7)□ Cla	aim(s) is/are objected to.						
8) <u></u> Cla	aim(s) are subject to restriction and/or	election requirement.					
Application Papers							
9) The specification is objected to by the Examiner.							
· · · · · · · · · · · · · · · · · · ·	10)⊠ The drawing(s) filed on <u>02 April 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a) ☐ All b) ☐ Some * c) ☐ None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
3. Copies of the certified copies of the priority documents have been received in this National Stage							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)							
	References Cited (PTO-892) Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail Da					
3) Information	on Disclosure Statement(s) (PTO-1449 or PTO/SB/08) (s)/Mail Date		atent Application (PTO-152)				

DETAILED ACTION

This is a response to the RCE filed 2/9/2006. Claims 9-16 are pending and are under examination.

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olisar et al. (USP 4,873,456) in view of a Japanese reference JP 5-37305.

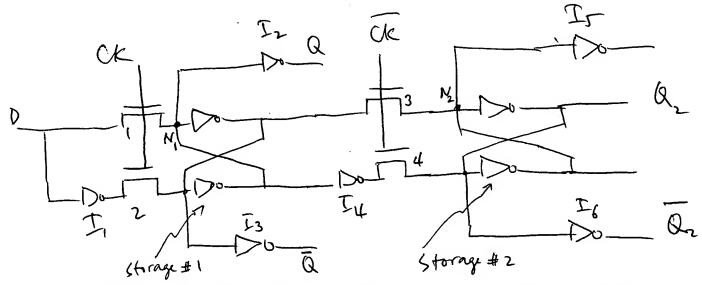
Figure 1 of Olisar et al. shows a configuration of a master-slave flip flips having two D flip flop circuits connected in series, wherein the master flip flop (12) and the slave flip flop are clocked a true and a complement clock signal.

Olisar et al. reference does not show the detailed structure of each D flip flop. Figure 1 of the Japanese reference JP 5-37305 shows a detailed structure of a D flip flop having time delay unchanged as the supply voltage changes. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to implement Olisar et al.'s D flip flop with JP 5-37305 D flip flop for the purpose of providing a constant time delay.

Below is the detailed arrangement of the combination of Olisar et al. and JP 5-37305 references. The combination of reference comprises an input signal (D), a first pass gate (1), a first storage node (N1), a second pass gate (3), a first inverter (I4), a third pass gate (4), an unclocked second storage node (N2) as called for in claim 9.

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Regarding claim 10, the combination of references shows a second inverter (I5) and a third inverter (I6).

Regarding claim 11, the combination of references shows the first storage node comprises two inverters.

Regarding claims 13, the combination of references shows the second storage node comprises two inverters.

Regarding claim 12, the combination of references shows fourth and fifth inverters (upper and lower inverters of the storage nodes) but does not disclose the sixth inverter is weaker than the fourth inverter. However, it is known to have the upper inverter of the master stage bigger than the upper inverter of the slave stage in order to overcome the signal of the subsequent stage (slave stage) thus preventing erroneous operation. Therefore, outside of an non-obvious results, the obviousness of having inverters of different size will not be patentable under 35USC 103(a).

Regarding claim 14, the combination of references shows does not disclose the fourth inverter (upper inverter of the second storage node) is weaker than the first inverter (I4).

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However, it is known to have the input inverter bigger than the inverters of the storage within the master or slave flip flop in order to overcome the signal within the latch thus preventing erroneous operation. Therefore, outside of an non-obvious results, the obviousness of having inverters of different size will not be patentable under 35USC 103(a).

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Regarding claims 15-16, since the first and second storages are not clocked storage, therefore, the stored input data and the inverted stored input data conveyed to the true and complement output nodes (Q2, Q2/) regardless of states of the master clock signal and the slave clock signal.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam Primary Examiner

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3/10/2006